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RESEARCH ARTICLE

HDL DESIGN FOR EXA HERTZ CLOCK BASED 2E31-1 EXA BITS PER SECOND (EBPS) PRBS DESIGN FOR ULTRA HIGH SPEED APPLICATIONS/PRODUCTS

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CCITT – Consulting Committee for International Telegraph & Telecom, ITU – International Telecom Unit, RTL- Register Transfer Level, LFSR-Linear Feedback Shift Register, VHDL- Very High Speed Integrated Circuit Hardware Description Language, PRBS-Pseudo Random Binary Sequence.

ABSTRACT

The Design is mainly Intended for High Speed Random Frequency Carrier Wave Generator of Exa Bits Per Second Ebps (Exa Bits Per Second) Data Rate $2e^{23}$-1 Tapped PRBS Pattern Sequence. The PRBS is Designed by using LFSR Linear Feed Back Shift Register and XOR Gate with Specific Tapping Points as per CCITT ITU Standards. RTL Design Architecture Implemented by using VHDL and/ Verilog HDL, Programming and Debugging Done by using Spartan III FPGA Kit. Transmission done through this carrier frequency. Propagation Carrier Done either Serially / Parallel lines I/O.

INTRODUCTION

In Modern Hi-tech Communication Engineering world, High Speed based Portable Communication System Hardware and Software Products Came to the market, speed is an important factor and is in terms of Giga bits per second for all Hi-tech Real time Smart Computing Portable wireless Communication System Software products like Cloud Computing, wireless Internet Data Packets Transceivers Computing, Tablets, Pocket Mobile Multimedia Systems, Note Book Computers, Wireless Routers, NOCs, Network Cards/Racks, WiFI, GiFi, Wimax, GPS, GSM, QCDMA Tranceivers.

For that purpose, I Designed Exa Bits Per Second High Speed PRBS is Pseudo Random Binary Sequence Frequency Generators, Generate and Received Random Frequency Data in the form of Random frequency numbers of different speed w.r.t specific data tapping sequence points for both signal and carrier wave generation. PRBS Generators, Receivers, Transceivers Designed for HiFi Wireless Internet Data Packets Computing and Cloud Computing etc. Transmission, Reception of Data is in the RANDOM Sense, This PRBS Generator, Receiver is Designed for Identification property of Different Tapped PRBS Sequences like 7,10,15,23,31 at a Clock carrier frequency speed of Ebps (Exa Bits Per Second).

The Length of PRBS sequence is 2^L-1. 2^L-1 times repeated the sequences. This is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like GPS Data Acquisition, GSM Communication Systems, WiFI, GiFI, LTE, Wireless OFDMA, CDMA, QCDMA Computing, wireless internet computing, cloud computing etc because of Ultra High speed Communication Rate in terms Tbps.

All these PRBS LFSR Sequences are designed by tapping different points according to ITU O.150, O.151,O.152 Standards. This PRBS Design Consists of Multiplexer, PRBS Registers of different tapped sequence points, Clock Frequency Generators of Ebps Speed. The Advantages of these PRBS Generators having In Built Checkers, Bit Error Rate Detection and Correction by using PRBS Checkers. These are simply Linear Polynomial Checkers and CRC.

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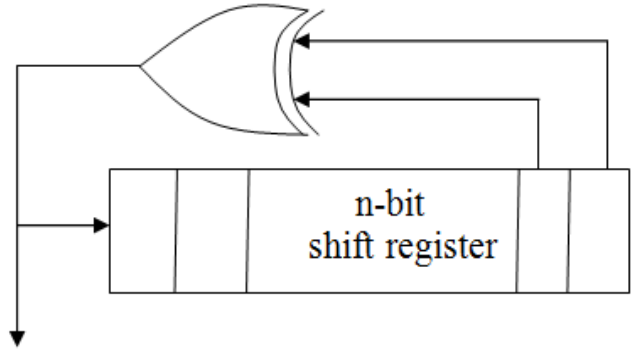
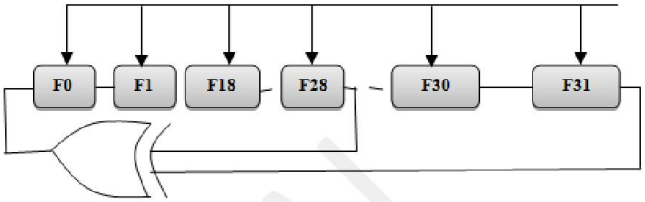


Fig. 1. Fibonacci (many-to-one) realization of LFSR with minimum number of taps and XOR gate in its feedback

$2e^{31}$-1 Exa Bits Per Second -Ebps- PRBS Design Ebps Clock



SOFTWARE – VLSI IC DESIGN FLOW

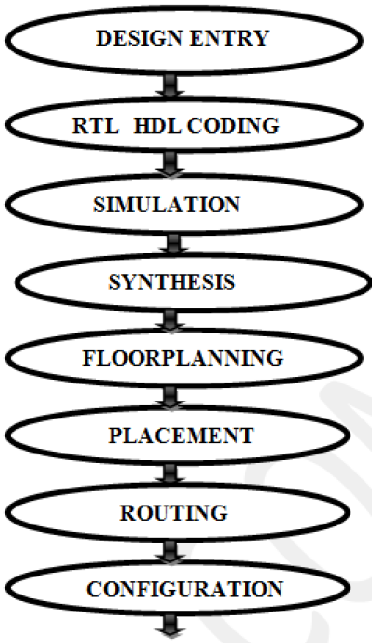
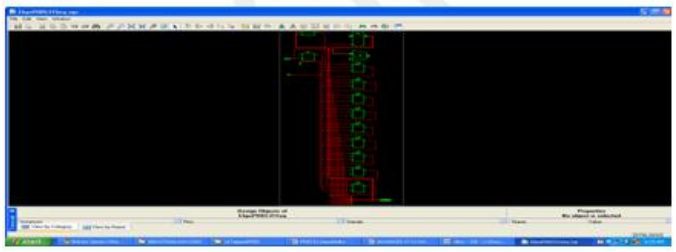


Fig. 3. VLSI Design Flow Chart

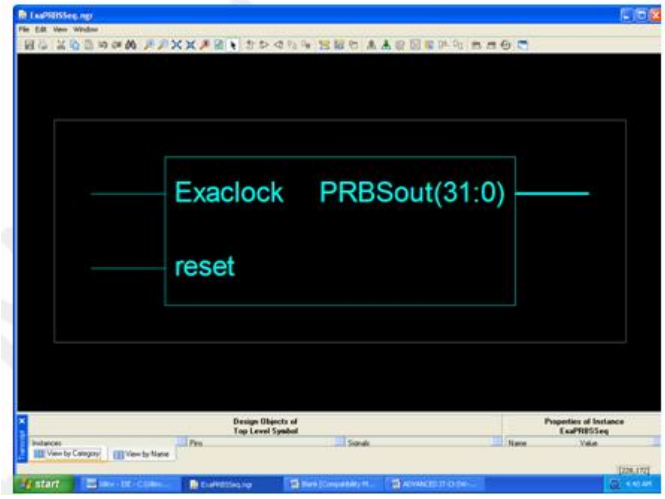
$2e^{31}$-1 Ebps PRBS RTL Schematic



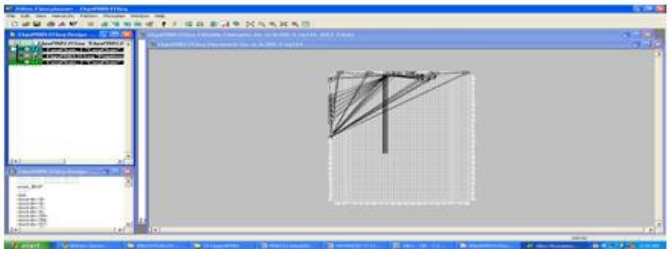
$2e^{31}$-1 Ebps PRBS DESIGN PLACED REPORT

DESIGN FLOW REPORTS OF $2e^{31}$-1 Ebps PRBS DESIGN

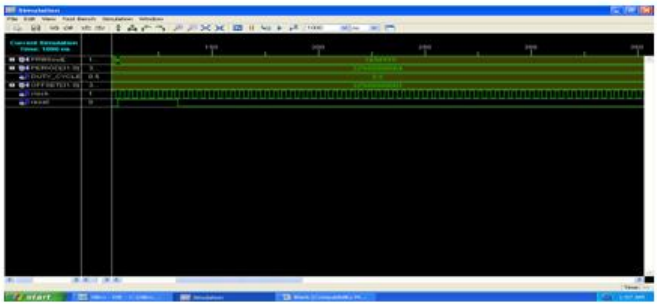
$2e^{31}$-1 Ebps PRBS DESIGN RTL BLOCK



$2e^{31}$-1 Ebps PRBS DESIGN ROUTED REPORT



SIMULATION WAVE FORM RESULTS -$2e^{31}$-1 Ebps PRBS



Conclusion

Designed High Speed Random Carrier Frequency Generator **$2e^{31}$-1 Ebps PRBS** for Ultra High Speed Wireless Communication Engineering Products

REFERENCES

[1] http://en.wikipedia.org/wiki/Pseudorandom_binary_ sequence

[2] "ITU-T Recommendations O151, O152 and O153," Tech. Rep.

[3] "https://www.verigy.com /help / topic /com." verigy.itee. help.smartest.ui.7.1.0/95305.html

[4] Xilinx Data Sheet XAPP884 (v1.0) January 10, 2011

[5] http://en.wikipedia.org/wiki/ Linear_feedback_shift_ register

[6] MAC WILLIAMS, FJ 1976, Pseudo Random Sequences & Arrays , IEEE Proc., 1715-1730 Ahmad, A., Nanda, N. K., and Garg, K., "An efficient design of maximal length of pseudorandom test pattern generators," *Proceedings of IEEE international conference on signals & systems,*

[7] Ahmad A. and Elabdalla A. M., "An efficient method to determine linear feedback connections in shift registers that generate maximal length pseudo-random up and down binary sequences," *Computer & Electrical Engineering - An Int'l Journal (USA),* vol. 23, no. 1, pp. 33-39, 1997.

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